Fabrication of a multilevel structure for nanophysics in two-dimensional electron gases

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The fabrication process of a multilevel structure with a central electrode isolated from the outer gates is presented. Polymethylmethacrylate is used as the dielectric material that provides the electrical isolation. Dot gates with a diameter as small as 30 nm aligned in the middle of 0.10 μm split gates have been fabricated. The operation of the dot gates has been tested by conductance measurements through the constriction formed by the split gates.

I. INTRODUCTION

High-mobility two-dimensional electron gas (2DEG) AlGaAs/GaAs heterostructure systems have been widely used for experiments in quantum transport at low temperatures.[1-7] Current microfabrication technology allows the fabrication of devices with a width W comparable to the Fermi wavelength l_F, length L shorter than both the elastic mean-free path L_e, and the phase-coherence length L_f of the carriers, and that leads to transport phenomena different from the classical regime, where $W \gg l_F$ and $L \gg L_e$, L_f.

A seminal experiment was the observation of quantized conductance (QC) steps in a ballistic point contact defined by split gates in a 2DEG.[8] Since then, the effect of impurities on the QC has been a problem that has been treated by several theorists[9-12] and experimental groups.[13,14] These experiments relied on scatterers naturally found in the constrictions. Instead, the introduction of an artificial scatterer in the ballistic constriction that can be turned on and off allows more control and thus a better understanding of the effect of impurities on the QC. Another interesting experiment that can be performed with a similar geometry is to observe interference of electron waves through a double slit, in addition to the observation of Fraunhofer diffraction[15] of electron waves through a single slit.

To perform the above experiments, it is necessary to have a small electrode that acts as the scatterer in the constriction or as the central electrode for the double slit. To tune the strength of the scattering potential or vary the separation between the double slits, it is necessary to connect the center electrodes to an external potential via a metal interconnect that does not affect the device. This is not possible using conventional planar lithographic techniques.[16] The aim of this paper is to describe a multilevel fabrication technique that can be used to fabricate such small electrodes in the middle of another set of gates. Polymethylmethacrylate (PMMA) is used as the dielectric material that isolates the middle gate from the outer gates. Since the central gate is fabricated in a lithography step separate from the outer gates, alignment is crucial for the device to be useful. A schematic diagram of the top view and the cross section of the multilevel structure is shown in Fig. 1.

II. DEVICE FABRICATION

The wafer used for the device fabrication is a molecular beam epitaxially grown GaAs/AlGaAs heterostructure, shown in Fig. 1, with a 2DEG at 49 nm from the surface. The fabrication process consists of seven lithography steps.

First, mesas that isolate the devices from each other are defined by optical lithography, with the photoresist acting as a mask for the wet chemical etching. The next step is to fabricate the Ohmic contacts patterned by optical lithography. Conventional Ohmic metal Ni/Au/Ge for n-type GaAs is deposited by thermal evaporation followed by metal lift-off and rapid thermal annealing at 420 °C for 15–30 s.

The third layer is to pattern the alignment marks that are used to e-beam write the outer gates (in our case the split gates that define the constriction) and to e-beam write the central gate (in our case the scatterer). These alignment marks are crosses of 3 μm width, and are written using e-beam lithography, which gives smoother alignment marks than those patterned by optical lithography. In our design, the outer gates and the central gates are written in separate lithography steps (as is described later), and both layers use the same alignment mark as a reference to locate the e beam relative to the existing structures. Therefore the smoothness of the alignment mark is essential to align the central gate to the outer gates with good accuracy. Roughness in the mark would introduce noise in the signals used to detect the position of the mark as the beam is scanned across it, and would cause error in the detection of its position. Since the resolution required for the e-beam alignment mark layer is not high, the thickness of the e-beam resist and the current of the e beam can be quite large. A 500 nm thick PMMA with 496 K molecular weight is used for the resist, which is baked at

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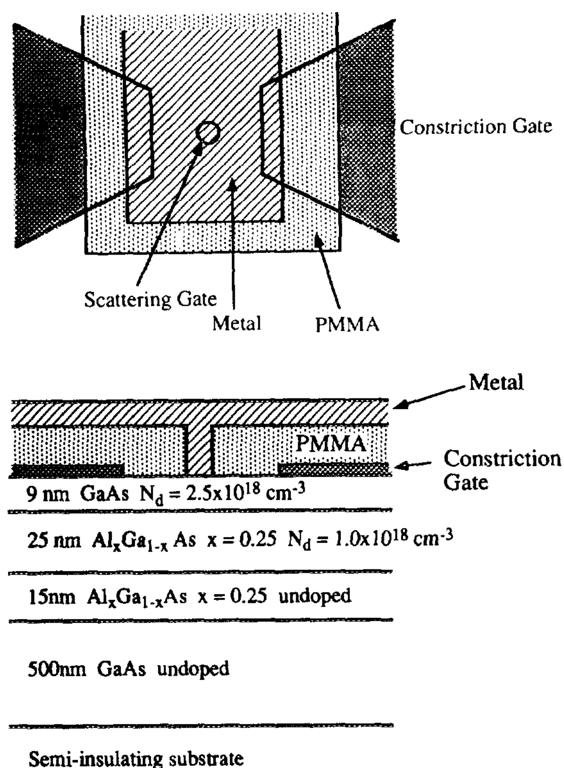

FIG. 1. (a) Top view of the multilevel structure with the scattering gate aligned in the middle of the constriction gates. (b) Cross-sectional view of the multilevel structure with the wafer structure. The scattering gate is defined by a window in the PMMA layer and the broad metal region, which serves as the interconnect of the scattering gate to the outside world is isolated from the constriction gates by the PMMA dielectric layer.

170 °C for 1 h, and the beam current is set around 2 nA. After the exposed PMMA is developed in methyl isobutyl ketone (MIBK): isopropyl alcohol (IPA) = 1:1 solution for 45 s, 5 nm of Cr followed by 150 nm of Au is thermally evaporated and lifted off.

The fourth layer is the fabrication of the outer gates using e-beam lithography. For the e-beam resist, a dual PMMA layer is used: a 50 nm thick Dupont Elvacite 2010 PMMA layer on the bottom followed by a 50 nm thick Dupont Elvacite 2041 PMMA layer on the top. Each layer is baked at 170 °C for 1 h. The bottom PMMA layer has a molecular weight of 100 K, which gives a higher sensitivity than the top PMMA layer with a molecular weight of 496 K, and therefore the resist profile has an undercut necessary for metal liftoff. After developing in MIBK:IPA = 1:3 at 21 °C for 45 s, 25 nm of Au/Pd alloy is deposited for the outer gate metal using thermal evaporation and then lifted off.

In the fifth lithography step the dielectric that provides isolation is spun on and windows for electrical contact are opened. For the dielectric a 100 nm thick 496 K molecular weight PMMA is used, and it is baked at 170 °C for 1 h. The windows of the dielectric are designed to overlap with the Ohmic contacts patterned in the second lithography step, and also with the gates patterned in the previous step. They are exposed by UV light and then developed in MIBK:IPA = 1:1. This exposure uses UV light instead of e beam for reasons of efficiency, since the features are large, and that would require

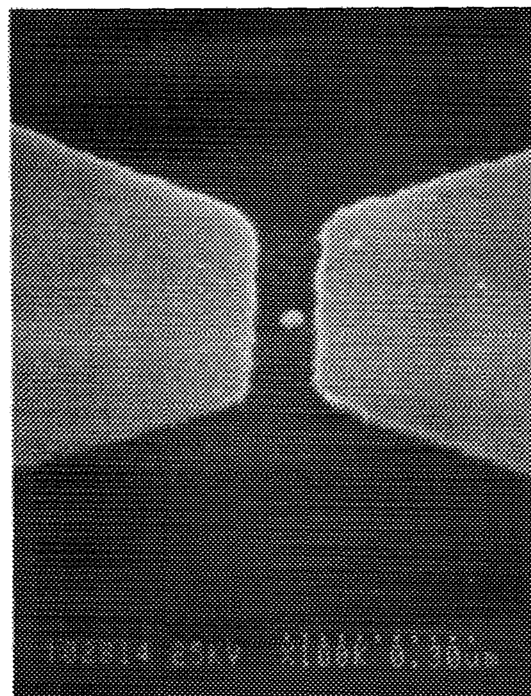

FIG. 2. A SEM micrograph of the scatterer in the middle of the constriction gates. This shows the good alignment achievable using our multilevel method. The diameter of the dot is less than 35 nm and the width of the constriction is 95 nm.

a long e-beam writing time. The sixth lithography step is to expose the central electrode by the e beam and then develop in MIBK:IPA = 1:3. Using PMMA as both the dielectric material and e-beam resist has the advantage of having a high resolution, and thus allows us to pattern central gates with very small dimensions. In our case, we have been able to form central electrodes with a diameter of 30 nm. Once the windows in the dielectric have been opened and the central gate defined, a thermal evaporation of the gate metal and bonding pad metal is done. Since the height/width aspect ratio of the central gate is quite large (>3), a metal with a small grain size is necessary in order to have a continuous gate from the top of the dielectric down to the surface of the wafer. Au/Pd is used because of its known small grain size. 80 nm of Au/Pd followed by 150 nm of Au is deposited. To visually confirm that the metal gets deposited on the surface of the wafer, and also to check the alignment of the center electrode to the outer gates, a separate deposition was done, where instead of filling the opening for the central gate all the way to the top, the Au/Pd deposition was stopped at 25 nm and followed by metal liftoff. Figure 2 shows a scanning electron microscope (SEM) micrograph of one of the typical structures observed. It is seen that the metal reaches the surface of the wafer, and also that the alignment is typically better than 30 nm.

The last lithography step is to etch the final metal layer to define the bonding pads for the different Ohmic contacts and gates. This is done using photoresist defined by optical lithography as a mask for the Au etchant. The Au etchant used is Gold Etchant Type TFA (Transene Company, Inc.), a complex aqueous solution that consists of 3% of an iodine

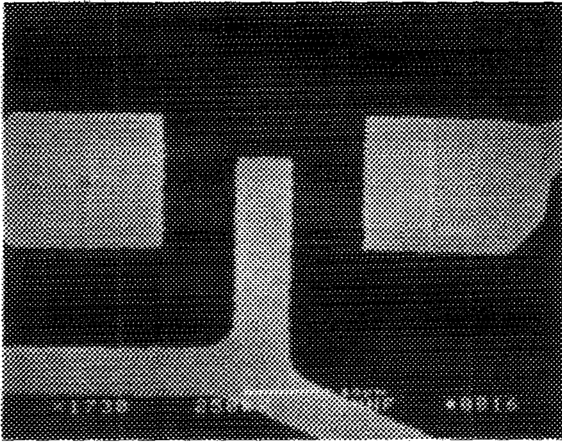

FIG. 3. A SEM micrograph of the central gate aligned to the outer gates. The dim metal regions are the two gates that form the constriction. The bright metal regions are the interconnects of the gates to the outside world defined at the last lithography step. The one in the middle is the interconnect of the central gate.

complex, 42% of potassium iodine, and water. This does not attack the PMMA layer and stops etching vertically once it reaches the PMMA layer. The photoresist mask is removed by flood exposure and development. A SEM micrograph of the central electrode on top of the outer electrodes is shown in Fig. 3. Here the bright regions are the electrical contacts in the final metal layer that were patterned using the etching method. The central gate contacts the surface of the wafer through the small opening in the PMMA layer that lies beneath. The large overlap of the central electrode area (10 μm wide) with the scattering gate is to provide suitable alignment tolerance for the optical lithography step. The dimly visible metal regions are the Au/Pd outer gates.

III. DEVICE CHARACTERIZATION

To confirm that the central gate is continuous from the top of the dielectric down to the surface of the wafer, an electrical test is done. If the metal is continuous, it should exhibit a Schottky diode characteristic. Figure 4 shows a $I-V$ char-

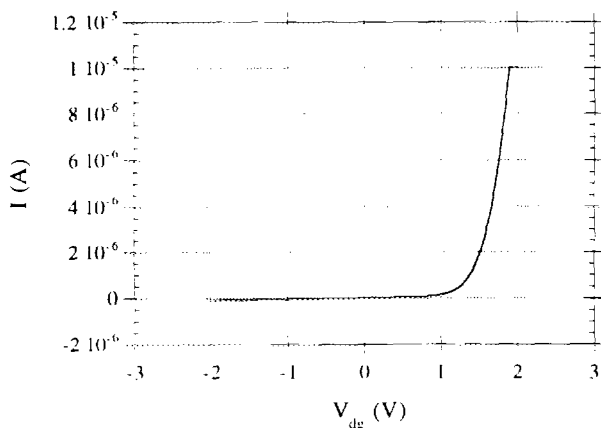

FIG. 4. $I-V$ characteristic of the dot gate showing a Schottky diode behavior.

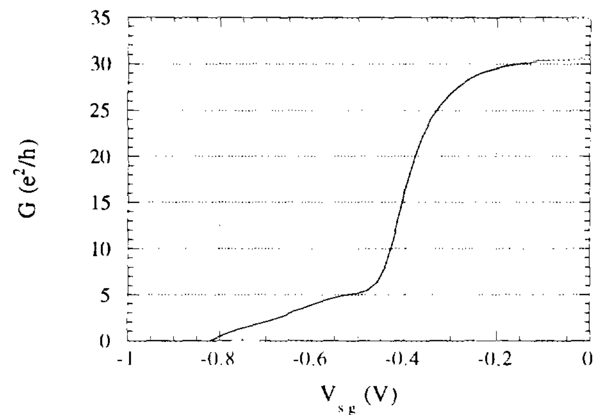

FIG. 5. Conductance through the constriction as the bias on the split gates, V_{sg}, is swept. The dot gate is left floating.

acteristic of the central gate at room temperature and confirms that it has the desired Schottky behavior.

Another way to check the operation of the central gate is to bias it and see its effect on the conductance along the channel defined by the split gates. A series of measurements of the conductance along the channel have been done at around 4 K using a lock-in amplifier to detect the low current level. First, a conventional conductance versus split gate voltage sweep was done to see the two different regimes: the two-dimensional (2D) regime and the one-dimensional (1D) tail, shown in Fig. 5. The dot gate was left floating during this sweep. The 2DEG threshold voltage is -0.48 V and the waveguide threshold voltage is -0.82 V. No quantized conductance steps are observed in this device. The carrier density and the mobility measured in the dark at 4 K were 2.5×10^{11} cm^{-2} and 1.38×10^{5} cm^2/V s, respectively. This, together with the 1.4 μm long constriction length, is the reason for the lack of observation of quantized conductance. The conductances are plotted in units of e^2/h to show that the values lie in the expected range and that the device performs as expected.

Next, a series of conductance versus dot gate voltage measurements, done with the split gate held at various bias voltage values, are shown in Fig. 6. It is seen that the central gate has a different influence on the conductance in the two regimes of the channel. When the split gate is biased to be in the 2D regime (the two curves on the top in Fig. 6, with $V_{sg}=-0.35$ and -0.40 V), the conductance along the channel cuts off at the same voltage -6.4 V, independent of the split gate bias. However, when the split gate is biased negatively enough to deplete the carriers underneath and define a 1D channel (the two curves on the bottom in Fig. 6 with $V_{sg}=-0.55$ and -0.75 V), the cutoff voltage increases as the split gate voltage decreases. Also, the shape of the curves differs from that in the 2D regime. In the transition between 2D and 1D regimes (curves with $V_{sg}=-0.40$, -0.42 and -0.46 V) there is a somewhat anomalous behavior, where the conductance first decreases until $V_{dg}\approx-3$ V and then remains nearly constant from $V_{dg}\approx-3$ V to the cutoff at -6.4 V.

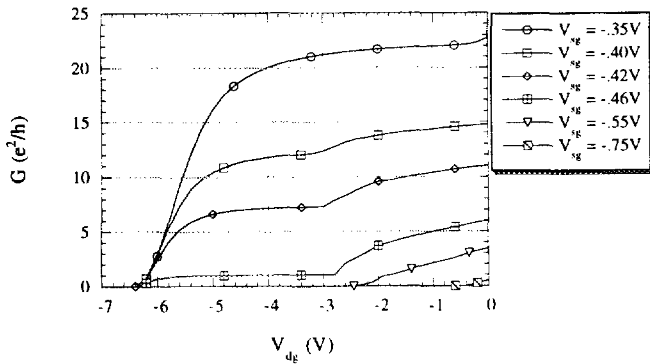

FIG. 6. Conductance vs dot gate voltage curves of the multilevel structure. The series of curves with different V_{sg} values show the conductance through the constriction as the dot gate bias, V_{dg}, is swept with a constant split gate voltage, V_{sg}. Plot symbols are for identification and do not represent all the data points.

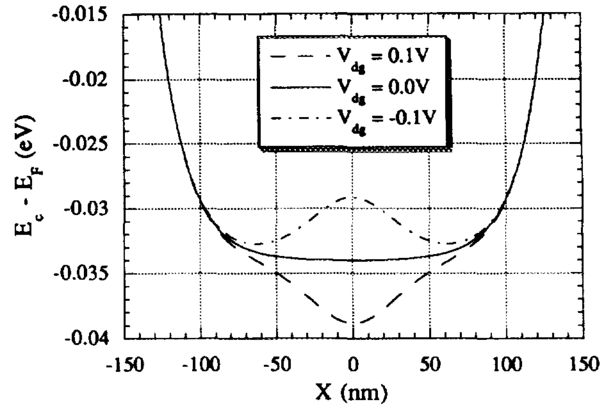

FIG. 7. Simulated energy band diagram of the structure of Fig. 1, at a depth of 50 nm. The split gate separation is 300 nm, and the dot diameter is 30 nm. The split gate bias is −0.5 V, and the dot gate biases are −0.1, 0.0, and 0.1 V.

We consider the above observations to be consistent with the presence of the small dot gate. In the 1D regime, the channel is narrow enough such that the shift of the conduction band due to the bias on the dot has a significant effect on the conductance along the channel. Therefore, the conductance will decrease monotonically as the bias voltage on the dot is decreased and eventually reach cutoff. The bias voltage that depletes the channel will depend on the width of the channel. The wider the channel the more negative the bias on the dot must be to cut off the channel. On the contrary, in the 2D regime, depleting the electrons beneath the 30 nm dot should not have any significant effect on the conductance since current flows through the full width of the 40 μm wide mesa. Therefore the dot gate will not modulate the conductance until the large-area electrode atop the PMMA starts to have an influence on the channel. Referring to Fig. 3, we see that there is a region away from the split gates, where the central electrode extends completely across the mesa, forming a metal–insulator–semiconductor (MIS) FET. The large-area electrode, or gate, cannot modulate the electron density in the 2DEG until it first overcomes the Fermi level pinning due to the surface states at the interface between the PMMA and the GaAs. Therefore the conductance remains nearly constant until a certain value of the dot gate voltage (≈ -4 or -5 V) and then decreases rapidly. This is consistent with the behavior of GaAs MISFETs.[17] The anomalous behavior of the conductance, shown in Fig. 6, when the split gates hold the structure in the transition between 2D and 1D regimes can be understood as follows. At these split gate biases the 1D channel is beginning to form and much of the current flows between the gates, but some fraction of the current can still flow beneath the gates. As the dot gate voltage is reduced, it reduces the electron concentration in the channel between the gates, and thereby the overall conductance through the device. At $V_{dg} \approx -3$ V, the Schottky barrier begins to break down and conduct current. The small area of the dot restricts the current to values that do not influence the overall conductance through the device, but the series resistance of the diode restricts the voltage modulation of the surface barrier. Thus the dot does not significantly reduce the electron concentration in the channel, and the conductance is constant until the MISFET gate depletes the electrons as in the 2D regime. In the 1D regime the channel can be completely cut off before the breakdown voltage is reached.

We have also investigated the structure of Fig. 1 using a 2D Poisson simulation program.[18] This program calculates the band structure and electron concentration distribution, and includes a model for the surface state charge. These simulations confirm our interpretation of the data in Fig. 6. According to the simulations, the portion of the dot gate lying atop the PMMA will not influence the 2DEG until the dot gate bias is well beyond that needed to produce the necessary scattering potential. Figure 7 shows the results of one set of simulations. The band diagram is plotted along a horizontal line just below the AlGaAs/GaAs heterojunction of Fig. 1, at the position of the 2DEG. A structure with a dot of 30 nm diam and split gate separation of 300 nm is shown for dot gate biases of −0.1, 0.0, and 0.1 V. The split gate voltage is set to −0.5 V. This shows that a dot gate bias of 0.1 V produces a 5 meV potential difference in the 2DEG, which is the energy range of interest for scatterers in QC experiments. Also, the diameter of the energy perturbation is approximately 45 nm, which indicates that it is possible to produce a perturbation that closely replicates the size of the surface dot.

IV. CONCLUSION

We have demonstrated the fabrication process of devices with a nanoscale central electrode isolated from the outer gates. Details of the multilevel structure that uses PMMA for the dielectric material to provide electrical isolation have also been presented. With the high resolution of PMMA, we have been able to fabricate central dot gates with a diameter as small as 30 nm aligned in the middle of 0.10 μm split gates. The operation of the dot gates has been confirmed by conductance measurements. PMMA is shown to be a suitable insulator for an interlevel dielectric. In our work it is especially so, since the scattering gate is operated at low biases in a QC experiment. The PMMA provides good isolation of the large central electrode from the split gates and the 2DEG, such that only the small dot but not the large area of the

electrode has an influence on the 2DEG at the bias voltages of interest. Even at the stronger biases required for the center electrode of a double slit experiment, a PMMA insulator is suitable, since the bias required for a surface gate to deplete the 2DEG is well below that needed for the gate atop the PMMA to influence the 2DEG. We believe that these dot gates can be applied to nanostructures to study quantum transport in 2DEG.

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